REMARKS

Summary of Amendments

In the specification, the abstract has been amended for editorial clarity—and meanwhile to remain 150 or fewer words—further to its replacement by the preliminary amendment of April 24, 2006.

Independent claims 3 and 4 have been amended to more particularly point out and distinctly claim the method of the present invention. Claims 5 and 6 have been amended for consistency with the revision made to claims 3 and 4 to clarify that the subject matter of the present invention as set forth in those claims is more correctly recited as a method of *processing*, rather than *manufacturing*, a GaN substrate.

New claims 7 and 8 have been added to recite GaN substrates as having been processed by the method recited in independent claim 3, while new claims 9 and 10 have been added to recite GaN substrates as having been processed by the method recited in independent claim 4. Claims 7-10 thus incorporate all of the limitations of their respective parent claims. And since claims 7 and 9 correspond to claim 1, while claims 8 and 10 correspond to claim 2, these new claims are fully supported by the other pending claims themselves.

Claims 1-10 thus are before the Office for consideration by the Examiner.

Claim Rejections – 35 U.S.C. § 112

Claim 3 was rejected for indefiniteness; in particular, the Office asked what the recitation "an etchant having no Ga-face and N-face selectivity" means.

Claim 3 has been amended to recite,

> A method of processing a gallium-nitride semiconductor substrate <u>having a complex of faces in which Ga is exposed, and faces in which N is exposed</u>, the method comprising:
> (. . .)
> wet etching . . . by means of an etchant <u>that is not selective for either the Ga or the N faces of the substrate</u>.

It is believed that by clarifying that a GaN substrate to which the claim 3 processing method is directed has *a complex of faces in which Ga is exposed, and faces in which N is exposed*, the recitation that the etchant utilized in the claimed wet-etching step is nonselective *for either the Ga or the N faces of the substrate* is more than sufficiently definite to meet the requirements under 35 U.S.C. § 112.

Claim Rejections – 35 U.S.C. § 103

{Although the letter from the Office communicating its May 4, 2007 action presents in Section 1 the rejections of claims 3 and 5 before presenting in Section 2 the rejection of claims 1, 2, 4 and 6, the rejections are written as though Section 2 should be read before Section 1. Hence, in the following, the rejections will be addressed in that order.}

- **Claims 1, 2, 4 and 6; Yanagisawa '271 in view of Mizuniwa et al. '157 as evidenced by Takeuchi et al. '715**

Claims 1, 2, 4 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,814,157 to Mizuniwa et al. in view of U.S. Pat. No. 5,919,715 to Takeuchi (miswritten even in the issued patent as "Tekeuchi") et al.

Independent claims 1 and 2, which each recite a GaN substrate free of metallic contaminants to an unprecedentedly reduced extent, have been rejected essentially over *Mizuniwa et al.* alone, with *Takeuchi et al.* being cited to demonstrate intended, and therefore predictable, use.

Specifically, in contrast to the manner in which the Office relies upon the Mizuniwa et al. patent in making the rejection—addressed below—of claims 3 and 5, in order to reject claims 1 and 2 the Office does not rely upon the specific cleaning process taught in *Mizuniwa et al.* but instead cites from the *background* of the Mizuniwa et al. patent. The *Mizuniwa et al.* background, discussing the cleaning of semiconductor substrates in general, summarizes the "RCA cleaning method," and states (column 1, lines 32-34),

> The use of [the RCA] method can reduce a surface concentration of an absorbed metallic contaminant such as iron or copper down to not more than 1×10^{10} atoms/cm^2.

At the link <**http://www.mines.edu/fs_home/cwolden/chen435/clean.htm**>, the Colorado School of Mines describes the RCA cleaning method as follows.

> Contaminants present on the surface of silicon wafers at the start of processing, or accumulated during processing, have to be removed at specific processing steps in order to obtain high performance and high reliability semiconductor devices, and to prevent contamination of process equipment . . . . The RCA clean is the industry standard for removing contaminants from wafers. Werner Kern developed the basic procedure in 1965 while working for RCA (Radio Corporation of America)—hence the name.

The RCA cleaning procedure has three major steps used sequentially:

> I) **Organic Clean:** Removal of insoluble organic contaminants with a 5 : 1 : 1 H_2O : H_2O_2 : NH_4OH solution.
> II) **Oxide Strip**: Removal of a thin silicon dioxide layer where metallic contaminants may [have] accumulated as a result of (I), using a diluted 50 : 1 H_2O : HF solution.
> III) **Ionic Clean**: Removal of ionic and heavy metal atomic contaminants using a solution of 6 : 1 : 1 H_2O : H_2O_2 : HCl.
>
> The RCA cleaning technique does not attack silicon, and only a very thin layer of silicon dioxide is removed (in II) in the process. The procedure was also designed to prevent replating of metal contaminants from solution back to the wafer's surface. When finished, the polished side should be specular with no residue.

The *Mizuniwa et al.* background describes the RCA method as being for cleaning "a semiconductor wafer." Claims 1 and 2 of the present application recite gallium-nitride semiconductor substrates. The Office cites *Takeuchi et al.* to demonstrate that persons skilled in the art would desire to clean GaN substrates. Thus, the Office's ground for rejecting claims 1 and 2 appears to be that a person skilled in the art would find it predictable to apply the RCA cleaning method to GaN substrates.

And in fact, it would appear that the gist of *Takeuchi et al.* is the idea of using, if not an RCA-derived, then at least an RCA-inspired, technique for cleaning III-nitride substrates. In column 2, lines 19-23 *Takeuchi et al.* state,

> The present invention is based on the experimental observation that hydrofluoric acid etchant systems such as those used for forming mirror surfaces on a silicon-based semiconductor act as an effective etchant for group III-nitride semiconductors.

It is important to distinguish what it is that the *Takeuchi et al.* and RCA methods are etching. The target of such etchant-based cleaning techniques is stated in the *Takeuchi et al.* background, in lines 25-26 of column 1: "If the (semiconductor) surface is not cleaned to remove any oxide that has formed on the surface, the contact resistance between an electrode and the semiconductor becomes large." In other words, the goal of the *Takeuchi et al.* cleaning method is the removal of *oxide layers* from III-nitride semiconductor surfaces.

And in fact the specification in the present application discusses the removal of gallium oxide from GaN. In the background, in paragraph [0014], the present specification, citing a paper by Bardwell et al. from the *Journal of Applied Physics*,

notes, "The authors put forward the mechanism by which the gallium oxide Ga_2O_3 is subsequently dissolved by the KOH."

Meanwhile, to clean group III-nitride semiconductors *Takeuchi et al.*, as quoted above, employs hydrofluoric acid (HF, synonymously termed "hydrogen fluoride"), which is also employed in the "Oxide Strip" step of the RCA technique, also quoted above. And as it turns out again, the present specification acknowledges this conventional cleaning means: Paragraph [0048] of the present specification reads in full,

> Hydrogen fluoride (HF) is suited to taking off silicon oxide (SiO_2), as is well known. The problem is metals (Fe, Cr, Ni, Mn, . . .) apart from metalloid silicon. Inasmuch as metals cling to the surface, *if the surface itself can be removed at a certain thickness, then these metals can also be removed*.

(Emphasis added.)

The present invention as recited in claims 1 and 2 clearly is *not* the achievement of what the present specification itself acknowledges is conventional—the achievement of the removal of *oxide layers* from III-nitride semiconductor. Rather, the present invention as recited in claims 1 and 2 is the removal to a particularly achieved extent of metallic contaminants clinging to the surface of GaN semiconductor substrates.

While *Mizuniwa et al.* is directed to removing metallic contaminants absorbed in the surface of semiconductor wafers, *Mizuniwa et al.* achieve their results on silicon, and their disclosure is only enabling for achieving this on silicon. *Mizuniwa et al.* is based on a Japanese priority application filed in May, 1995—right at the time Shuji Nakamura of Nichia Corp. had experimentally achieved the first working devices on GaN substrates. Hence, *Mizuniwa et al.* dates to well before producing GaN substrates commercially was even a possibility.

It is noteworthy that the Colorado School of Mines description states, "The RCA cleaning technique does not attack silicon." Yet as stated as a goal in the above-quoted paragraph [0048] of the specification, the present invention removes the substrate surface itself to a certain thickness—in other words, the present-invention technique "attacks" GaN.

And although *Takeuchi et al.* may have shown that it is obvious to try an RCA-derived cleaning technique on III-nitride semiconductor substrates, the predictable result is that the *Takeuchi et al.* technique only removes oxide film, not surface-absorbed metallic contaminants. Again, in paragraph [0048] the present specification acknowledges this shortcoming. And again, the present invention in

contrast involves the realization that corrosively removing a slight amount of the GaN surface—which is counter to the teaching of the RCA technique, and by extension, *Mizuniwa et al.* and *Takeuchi et al.*—cleans it of metal contamination.

It might be countered that while the RCA cleaning method removes metallic contaminants by removing the oxide layer (cf. "oxide strip" step), the *Mizuniwa et al.* technique is not the RCA itself, but an improvement of the RCA technique, and consequently it should be asked how *Mizuniwa et al.* achieves removal of metallic contaminants, because the *Mizuniwa et al.* technique may "attack" the silicon substrate being cleaned.

Mizuniwa et al. employs, in solution at a specified pH, a chloric compound that acts as an oxidant to promote "dissolution of metallic and organic contaminations by acid, thereby . . . to remove organic and metallic contaminations from a surface of the solid-state material" (quoted from column 3, lines 48-52 specifically, repeated similarly throughout the Mizuniwa et al. disclosure). Yet it is never clear from *Mizuniwa et al.* whether the *Mizuniwa et al.* cleaning process actually attacks or eats away at the silicon. Regardless of *Mizuniwa et al.*'s silence as to the surface action of its process, as the present specification makes clear, etching III-nitride is a completely different consideration (is not possible with the wet etchants that work on silicon).

Finally, it should be noted that the Takeuchi et al. disclosure is completely mum as to the degree of cleanness achieved by the Takeuchi et al. technique. This is because the most that *Takeuchi et al.* can hope to remove as far as metal contaminants are concerned—an issue never mentioned by *Takeuchi et al.*—is any that may have accumulated in the oxide film itself, as is the case with the RCA cleaning method.

In sum, the present specification already acknowledges the combination that the Office has cited in rejecting claims 1 and 2. The present invention is directed to overcoming the problems the present invention realizes exist with *Mizuniwa et al.* and *Takeuchi et al.*, and similar technology. A person skilled in the art availing him or herself of either the Mizuniwa et al. disclosure or the Takeuchi et al. disclosure in view of the other would only have a reason to use the wet etch techniques disclosed in either reference to remove oxide from nitride semiconductor substrates. The present invention, in contradistinction to *Mizuniwa et al.* and *Takeuchi et al.*, and similar technology, removes not just metallically contaminated oxide-film residue on, but metallic contaminants absorbed into, the surface of the GaN substrate being cleaned. The present invention involves the realization that corrosively removing a slight amount of the GaN surface itself rids it of surface-absorbed metallic contaminants to an unprecedented extent.

The prior art of record does not disclose, teach, or suggest a *gallium-nitride* semiconductor substrate, as recited in claims 1 and 2, cleaned of surface metal contaminants to a 10×10^{11} atoms/cm^2 or lower density.

With regard to the rejection of claim 4, it is believed that the foregoing arguments are equally applicable, in that the conclusion that must be drawn is that the *Mizuniwa et al.* and *Takeuchi et al.* combination cannot lead to the present invention's achieving the removal to a predetermined thickness of the surface of the GaN substrate itself.

What is more, claim 4 now recites,

> A method of processing a gallium-nitride semiconductor substrate having a complex of faces in which Ga is exposed and faces in which N is exposed, the method comprising at least the step of:
> wet etching the substrate by means of an etchant that is one of $HF + H_2O_2$, $HCl + H_2O_2$, $H_2SO_4 + H_2O_2$, $HNO_3 + H_2O_2$, $HF + O_3$, $HCl + O_3$, $H_2SO_4 + O_3$, HNO_3, or $HNO_3 + O_3$, and that has an oxidation-reduction potential of more than 1.2 V.

Neither *Mizuniwa et al.* and *Takeuchi et al.*, nor any other prior art of record is dirtected to cleaning GaN substrates having a complex of faces in which Ga is exposed and faces in which N is exposed, nor by a wet etching process by means of a given etchant that has an oxidation-reduction potential of more than 1.2 V.

- **Claims 3 and 5; Yanagisawa '271 in view of Mizuniwa et al. '157 as evidenced by Takeuchi et al. '715**

Claims 3 and 5 were rejected as being unpatentable over U.S. Pat. App. Pub. No. 2001/0018271 to Yanagisawa in view of *Mizuniwa et al.* as evidenced by *Takeuchi et al*.

In rejecting claim 3, the Office cites *Yanagisawa* to demonstrate prior-art teaching of halogen plasma dry-etching of a semiconductor substrate to remove the "deteriorated layer" resulting from a planarizing process carried out on the substrate, and cites *Mizuniwa et al.* to demonstrate prior-art teaching of cleaning a semiconductor substrate by wet-etching it under certain conditions calculated to remove metal contaminants.

Here as well the Office cites *Takeuchi et al.* to give evidence of the art-recognized need to remove contaminants from group III-nitride semiconductor substrates. But as noted above in addressing the rejections of claims 1, 2, 4 and 6, the contaminants discussed in *Takeuchi et al.* are not metallic matter, but oxides of the substrate itself.

With particular regard to method claim 3, it is respectfully pointed out that the Office has not demonstrated that wet-etching removal of metallic contamination (*Mizuniwa et al.*) remaining after a (post-mechanical-polishing) dry etching process to remove a deteriorated layer (*Yanagisawa*) is predictable, because *Takeuchi et al.* is directed not to removing metallic residues as in the present invention, but to removing oxides of the substrate itself, as discussed at length in the foregoing.

More important, even if it would be predictable for a person skilled in the art to combine the teachings of *Yanagisawa* and *Mizuniwa et al.*, doing so would not lead to the present invention, for at least the following reasons.

- As the Office acknowledges, *Yanagisawa* does not teach halogen-plasma dry etching on gallium nitride, but rather on silicon. A yet further difference, overlooked by the Office, is that the plasma etching taught by *Yanagisawa* expressly uses a "neutral active species" which *by definition* is not ionic. Dry etching according to the present invention is, in contrast, reactive *ion* etching.

- The cleaning process taught in *Mizuniwa et al.* stipulates a cleaning solution that has an oxidation-reduction potential in the range of 800 mV to an *upper limit* of 1200 mV, because

  > if the oxidation-reduction potential is more than 1200 mV . . . at a temperature 25°C, an insufficient increase in cleaning power of the cleaning solution is obtained, even when the oxidation-reduction potential is sufficiently high

  (column 4, lines 25-30).

  In the present invention, the etchant is predetermined to have an oxidation-reduction potential of 1.2 V or greater, with Table II setting forth some combinations of etchant ingredients found to achieve an oxidation-reduction potential of greater than 1.2 V.

  Claim 3 has been amended to recite

  > A method of processing a gallium-nitride semiconductor substrate <u>having a complex of faces in which Ga is exposed and faces in which N is exposed</u>, the method comprising:
  > <u>polishing the substrate with an abrasive embedded into a metallic platen, thereby leaving a process-transformed layer on the substrate;</u>
  > <u>reactive-ion etching the substrate using a halogen plasma</u> to remove the process-transformed layer; and

wet etching the reactive-ion etched substrate, by means of an etchant that is not selective for either the Ga or the N faces of the substrate, yet does have metal etching capability, and an oxidation-reduction potential of more than 1.2 V, thereby to remove contaminant metal produced by said reactive-ion etching.

It is respectfully submitted that combination of *Yanagisawa* and *Mizuniwa et al.* does not arrive at the combination of steps now recited in claim 3, performed on a GaN substrate as recited in the claim 3 preamble.

Conclusion

For the foregoing reasons independent claims 1 through 4 are believed to be allowable over the prior art of record. Thus it is also believed that claims 5 and 6, as well as new claims 7-10, which depend directly from, and properly contain all of the limitations of, either claim 3 or claim 4, should be held allowable over the prior art of record.

Accordingly, Applicant courteously urges that this application is in condition for allowance. Reconsideration and withdrawal of the rejections is requested. Favorable action by the Examiner at an early date is solicited.

Respectfully submitted,

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/James Judge/

James W. Judge
Registration No. 42,701

JUDGE & MURAKAMI IP ASSOCIATES
Dojima Building, 7th Floor
6-8 Nishitemma 2-Chome, Kita-ku
Osaka-shi 530-0047
JAPAN

Telephone: **305-938-7119**
Voicemail/Fax: **703-997-4565**